



# **Reliability Report**

**Reliability Data for Low Voltage Optically Triggered Phototransistors  
and Photodiodes 30V – 100V**

**Report Title: Reliability Data for Low Voltage Optically Triggered  
Phototransistors and Photodiodes 30V – 100V**

**Report Number: 2014-005**

**Date: 6/17/14**

**Reliability Report-Low Voltage Optically Triggered Phototransistors and Photodiodes  
30V – 100V  
Qualification No: 2014-005**

**Introduction:**

This report summarizes the Reliability data of IXYS Integrated Circuits Division Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V (represented by LDA100). The Reliability data presented here were collected during IXYS product qualification. The purpose of this qualification was to verify the IXYS Quality and Reliability requirements as outlined in IXYS internal specifications. The LDA100 silicon is manufactured using the P4.0 process at IXYS Integrated Circuits Division in Beverly, MA USA and assembled at Atec in the Philippines.

**Reliability Tests:**

Table 1 below provides the qualification tests that were performed. The stress tests and sample size are chosen based on the IXYS internal specification and with the approval of the product development team and quality assurance.

**Table 1: Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V Reliability Tests**

Stress Test	Applicable Specs	Stress Conditions	Product/ Package	Number of Lots	Sample Size (SS)	Total SS
HTOL	Mil-Std-883	125°C, 80%	LDA100 6 Pin DIP	1	105	105
Thermal Shock (T/S)	Mil-Std-883, M1011	0 to 100°C, 10/10 dwells, 15 cycles	LDA100 6 Pin DIP	1	55	55
Temp Cycle (T/C)	Mil-Std-883, N1010, “B”	-55 to 125°C, 10/10 dwells, 300 cycles	LDA100 6 Pin DIP	1	55	55
High Temp Storage	JESD22-A103C	150°C, 1000hrs	LDA100 6 Pin DIP	1	45	45
MSL	J-STD-020D.1	IR Reflow, Level 1	LDA100 6 Pin DIP	1	25	25
ESD HBM	JESD22, A114-E	1.5kΩ, 100pF	LDA100 6 Pin DIP	1	3	3

**Reliability Report-Low Voltage Optically Triggered Phototransistors and Photodiodes  
30V – 100V  
Qualification No: 2014-005**

**Reliability Test Results:**

The stress tests and associated results for the product Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V qualification are summarized in Table 2. The devices chosen for the qualification were from standard material manufactured through normal production test flow and electrically tested to datasheet limits prior to stressing. Then reliability stresses were conducted and electrically tested to datasheet limit at each interval and final readpoints.

**Table 2: Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V Reliability Test Results**

<b>Stress Test</b>	<b>Product/Kit Number</b>	<b>Readpoint / (Reject/ SS)</b>
HTOL	LDA100 T62582	1000 hrs.
		0/105
Thermal Shock	LDA100 T62582	15 Cycles
		0/55
Temp Cycle	LDA100 T62582	300 Cycles
		0/55
High Temp Storage	LDA100 T62582	1000 hrs.
		0/45
MSL	LDA100 T62582	IR Reflow Level 1
		0/25

**ESD Testing Results:**

As part of this qualification, the product Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V was subjected to Human Body Model (HBM) ESD Sensitivity

**Reliability Report-Low Voltage Optically Triggered Phototransistors and Photodiodes  
30V – 100V  
Qualification No: 2014-005**

Classification testing using a KeyTek Zapmaster system. The results are summarized in Table 3. All samples were electrically tested to data sheet limits before and after ESD stressing and they passed after +/-6500V testing.

**Table3: Low Voltage Optically Triggered Phototransistors and Photodiodes  
30V – 100V**

**ESD Characterization Results**

<b>ESD Model</b>	<b>Product/Kit Number</b>	<b>Package</b>	<b>ESD Test Spec</b>	<b>RC Network</b>	<b>Highest Passed</b>	<b>Class</b>
HBM	LDA100 T62582	6 Pin DIP	JESD22, A114-E	1.5kΩ, 100pF	6500V	3A

**FIT (Failure in Time) Rate on the Product Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V:**

Table 4 summarizes the number of devices used for the product Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V reliability stress with associated failures. Using the HTOL data, FITs were calculated based on the Acceleration Factor (AF) and equivalent device hours at 0.7eV of activation energy for 125°C test temperature and 40°C use temperatures. The calculated FITs from the reliability stress came out to be 34.31 for HTOL.

**Table 4: Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V FIT Rate Summary**

<b>Qual#</b>	<b>Stress</b>	<b>Product/Kit Number</b>	<b># of Devices</b>	<b># of Fails</b>	<b>Hours Tested</b>	<b>Act. Energy</b>	<b>Acc. Factor</b>	<b>Equivalent Dev. Hours</b>	<b>FIT Rate @ 60% CL</b>
1	HTOL	LDA100 T62582	105	0	1000	0.7	255.41	26,817,626	34.31

**Reliability Report-Low Voltage Optically Triggered Phototransistors and Photodiodes  
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## **Conclusion:**

The qualification of the product Low Voltage Optically Triggered Phototransistors and Photodiodes 30V – 100V has been successfully completed for the production release.

## **APPROVAL:**

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